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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,902	08/11/2000	Kozo Harada	50090-234	8376

7590 05/02/2003

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EXAMINER
CHU, CHRIS C

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/635,902	HARADA ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4, 6, 9 and 12 ~ 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4, 6, 9 and 12 ~ 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on February 19, 2003 has been received and entered in the case.

Claim Objections

2. Claims 6, 17 and 18 are objected to because of the following informalities:

In claim 6, line 13, "or insulation layer' should be --or said insulation layer--.

Since claims 17 and 18 are dependent claims of cancelled claims, claims 17 and 18 need a correction.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Seidler.

Regarding claim 12, Seidler discloses in Fig. 8 a semiconductor device comprising:

- a plurality of semiconductor device units, each of said semiconductor device units including:
    - a semiconductor chip (260);
    - at least a first electrode (262) formed on the first major surface of said semiconductor chip,
    - at least a second electrode (264) or an insulation layer formed on the second major surface opposite to said first major surface; and
    - at least a conductive member (210) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;
    - a packaging board (260') for mounting said plurality of semiconductor device units;

- wherein said semiconductor device units are placed on said packing board so as to have a predetermined angle to said packaging board, and said conductive members of said semiconductor device units are connected to said packaging board,
- wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer, said conductive clip having elasticity for clamping objects.

5. Claims 4, 9 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsubosaki et al.

Regarding claim 4, Tsubosaki et al. discloses in Fig. 9 a semiconductor device comprising:

- a semiconductor chip (1);
- at least a first electrode (4) formed on the first major surface of said semiconductor chip,
- at least a second electrode or an insulation layer (7) formed on the second major surface opposite to said first major surface; and
- at least a conductive member (3) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip,
- wherein each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said

second electrode or said insulation layer such that at least a portion of said conductive layer contacts said surface.

Regarding claim 9, Tsubosaki et al. discloses in Figs. 14 and 15 a semiconductor device comprising:

- a plurality of semiconductor device units (20), each of said semiconductor device units including:
    - a semiconductor chip (1);
    - at least a first electrode (4) formed on the first major surface of said semiconductor chip,
    - at least a second electrode or an insulation layer (7) formed on the second major surface opposite to said first major surface; and
    - at least a conductive member (3) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;
    - wherein said semiconductor device units are stacked on each other, and said conductive members are connected to each other,
    - wherein each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer such that at least a portion of said conductive layer contacts said surface.

Regarding claim 13, Tsubosaki et al. discloses in Figs. 14 and 15 a semiconductor device comprising:

- a plurality of semiconductor device units (20), each of said semiconductor device units including:
    - a semiconductor chip (1);
    - at least a first electrode (4) formed on the first major surface of said semiconductor chip,
    - at least a second electrode or an insulation layer (7) formed on the second major surface opposite to said first major surface; and
    - at least a conductive member (3) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;
    - a packaging board (21) for mounting said plurality of semiconductor device units;
    - wherein said semiconductor device units are placed on said packaging board so as to have a predetermined angle to said packaging board, and said conductive members of said semiconductor device units are connected to said packaging board,
    - wherein each of said conductive members is comprised of a conductive layer formed on the surface of said semiconductor chip extending from said first

electrode to said second electrode or said insulation layer such that at least a portion of said conductive layer contacts said surface.

6. Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Eide.

Eide discloses in Fig. 6a, Fig. 7 and column 3, lines 41 ~ 43 a semiconductor device comprising:

- a plurality of semiconductor device units, each of said semiconductor device units including:
    - a semiconductor chip (8);
    - at least a first electrode (under 10, the top) formed on the first major surface of said semiconductor chip,
    - at least a second electrode or an insulation layer (under 10, the bottom) formed on the second major surface opposite to said first major surface; and
    - at least a conductive member (10) for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;
    - wherein said semiconductor device units are stacked on each other,
    - wherein a first chip has a first conducting pattern (under 5, the top) extended from said first electrode, a second chip has a second conducting pattern (under 5, the bottom) extended from said second electrodes or insulation layer, and a bump (5) is provided between said first conducting pattern and said second

conducting pattern, which face to each other, for electrically connecting said two conducting patterns.

7. Claims 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Bertin et al.

Regarding claim 14, Bertin et al. discloses in Fig. 17, Fig. 18 and column 6, lines 35 ~ 44 a semiconductor device comprising:

- a plurality of semiconductor chips (40A) each having electrodes formed on the major surface thereof, and
- a plurality of spacer members (88C) each having a conductive pattern on the surface thereof;
- wherein each of said plurality of semiconductor chips has first and second opposing side surfaces arranged adjacent to first and second spacer members of said plurality of spacer members, respectively;
- wherein said semiconductor chips and said spacer members are stacked alternately such that said electrodes of said semiconductor chips directly contact corresponding conductive patterns at a portion of the corresponding conductive patterns formed on the surface of the spacer member and are electrically connected to said conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other.

Regarding claim 15, Bertin et al. discloses in Figs. 17 and 18 each of said spacer members having a cavity for accommodating the end portion of said semiconductor chip, said end portion is located at least partially within the cavity.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bertin et al. in view of Miyoshi.

Bertin et al. discloses the claimed invention except for supporting members. However, Miyoshi teaches in Fig. 18 supporting members (61) having conductive pattern (47e, 47f, 47g and 47j) thereon, wherein said supporting members are placed so as to make said conductive patterns thereof contact with said conductive patterns of said plurality of spacer members. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bertin et al. by using the supporting members as taught by Miyoshi. The ordinary artisan would have been motivated to modify Bertin et al. in the manner described above for at least the purpose of mounting a plurality of semiconductor chips as being horizontally laminated in a predetermined spacing (column 8, lines 48 and 49).

10. Claims 17 ~ 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seidler in view of Kitahara.

Regarding claims 17 ~ 19, Seidler discloses the claimed invention except for the conductive member including a first conductive end which contacts the first electrode, and a second conductive end which contacts the second electrode or the insulation layer. However, Kitahara teaches in Fig. 8(b) and column 2, lines 31 ~ 38 the conductive member (3) including a first conductive end (31) which contacts the first electrode (11), and a second conductive end (35) which contacts the second electrode or the insulation layer (5). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Seidler by using the supporting members as taught by Kitahara. The ordinary artisan would have been motivated to modify Seidler in the manner described above for at least the purpose of increasing structural strength (column 3, lines 1 and 2).

Response to Arguments

11. Applicant's arguments filed on February 19, 2003 have been fully considered but they are not persuasive.

On page 7, applicant argues "Seidler does not disclose or suggest, *inter alia*, 'a packaging board for mounting said plurality of semiconductor device units', it is submintted that Seidler does not anticipated claim 12." This argument is not persuasive. Seidler discloses in column 6, lines 28 ~ 40 and column 7, lines 9 ~ 16 the lead 210 may be extended as at 216 for connection to other electrical elements. This sentence clearly indicates that Seidler has a plurality of semiconductor device units as recited in lines 4 – 11 of claim 12 and a packaging board.

Further, applicant argues "there is nothing in Seidler that suggests clip 10 MUST clamp the opposing pads 62 and 64 together." This argument is not persuasive. The dictionary definition of clip is as follows:

To hold in a tight grip: CLUTCH

(Merriam-Webster's)

Since the clip 10 of Seidler presses the contact pads 62 and 64 together so as to hold them firmly, the clip 10 of Seidler has elasticity for clamping objects as recited in claim 12.

Therefore, Seidler anticipates claim 12.

On page 9, applicant argues "Tsubosaki et al. does not disclose or suggest, *inter alia*, a 'conductive layer formed on the **surface** of said semiconductor chip' as recited in each of claims 4, 9 and 13, it is submitted that Tsubosaki et al. does not anticipate claims 4, 9 and 13." This argument is not persuasive. Tsubosaki et al. clearly shows in Fig. 14 and Fig. 15 a conductive layer (3) formed on the surface (an area where 3 is attached to element 2) of said semiconductor chip (1).

On page 10, applicant argues "Eide is completely silent as to what is formed on the TSOP chips 8 ... the TSOP chips 8 do NOT necessarily have **both** electrodes **and** conducting patterns under the conductive elements 5, 10 in the manner recited in claim 6." This argument is not persuasive. Eide discloses in column 4, lines 31 ~ 40 the TSOP chips 8 having I/O terminals thereon and a flexible circuit.

Finally, applicant argues "Eide is ... completely silent as to the relative arrangement of electrodes and/or conductive patterns on the chips themselves ... the conductive patterns extending from the electrodes, let alone patterns which face each other on opposing chips and which are connected via a bump in the manner recited in claim 6." This argument is not persuasive. Eide discloses in Figs. 3 ~ 7 the conductive patterns (7 in Fig. 3, under 5 in Fig. 7) extending from the electrodes (under 10), let alone patterns (C and D) which face each other on opposing chips (A and B) and which are connected via a bump (5).

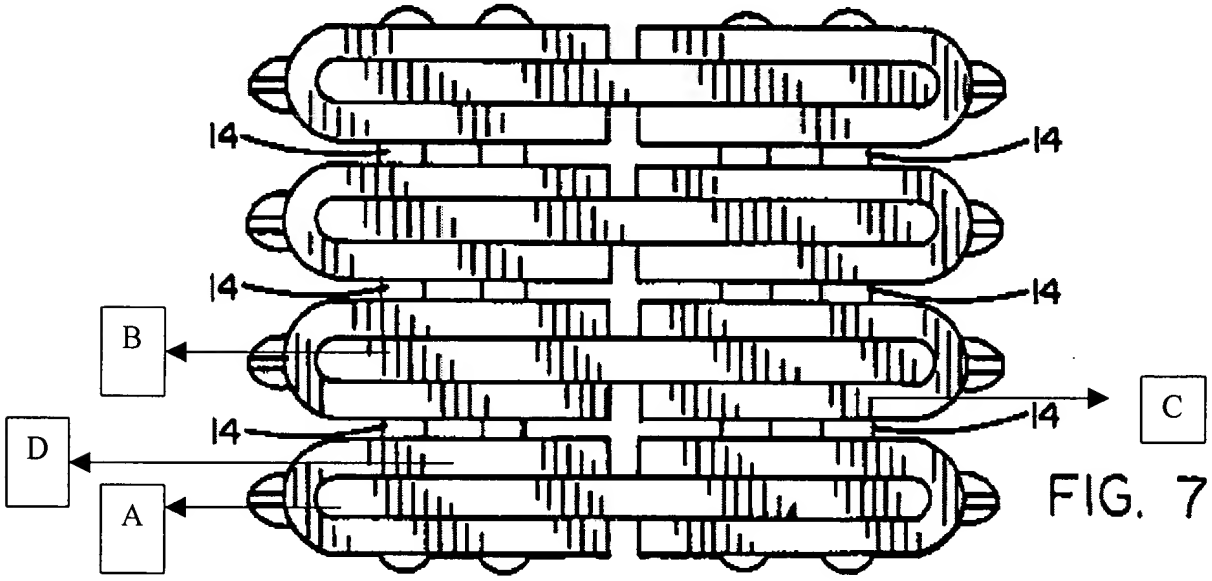

FIG. 7

For the above reasons, the rejection is maintained.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
April 29, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800